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Performance analysis of a DRL-less AFE for battery-powered wearable EEG

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ABSTRACT

The driven-right-leg (DRL) circuit has been commonly used in the wall-powered EEG systems to reduce common-mode interference in the bio-potential amplifier. However, DRL circuit imposes limitations on the number of channels preventing modular development, and its effectiveness is diminished for a newer generation of battery-powered EEG systems. We present a performance investigation of DRL-less EEG circuit by designing a single-channel EEG with a novel Analog Front End (AFE) that contains a differential amplifier followed by a high-Q active notch filter. The prototyped wearable EEG system has been validated to record neural signals with and without the DRL circuit. The time domain and frequency domain signals show that the designed AFE is not impacted significantly (maximum 4 dB difference) by the DRL elimination and maintains similar signal quality. The customized EEG with and without DRL offers CMRR of 72.98 dB and 71.74 dB, respectively, at 60 Hz (power-line interference range in the USA), whereas CMRR of 72.64 dB and 71.01 dB, respectively, at 20 Hz (representative EEG signal range). DRL elimination allows us to envision a sensor-level modular EEG system for neural monitoring in non-clinical environments.

1. Introduction

For neurological signal recording, Electroencephalography (EEG) is a suitable non-invasive technology to monitor patients outside of clinical settings. Compared to Magnetoencephalography (MEG), Functional Magnetic Resonance Imaging (FMRI) and Positron Emission Tomography (PET) techniques, EEG sensors are miniature, lightweight, and low-cost; hence, they can be conveniently worn for continuous sensing of brain activities at natural environments [1–3]. Though there is a plethora of research on designing wireless EEG measurement tools using commercial-off-the-shelf (COTS) components and custom-fabricating ICs [4–13], little attention has been provided for a modular EEG device with plug-and-play sensors. Battery-powered ambulatory, easily deployable and modular devices that integrate multiple sensors are critically important especially for diagnosis and therapy assessments of patients with neurological disorders (e.g. Alzheimer's, Autism Spectrum Disorder, Post-Traumatic Stress Disorder, and Attention Deficit Hyperactivity Disorder), and monitoring of elderly, emergency care patients, and soldiers in the battlefield for vitality signs [14–17].

The recordings from wearable EEG systems are severely affected by power-line interference. This interference in bio-potential recordings must be suppressed, as they can overwhelm the significant features of interest of the signal. Also, for the wall power supplied EEG systems, as the power lines are earth grounded, displacement currents coupled to the electrodes flow through the patient to earth. These displacement currents can lead to develop common mode voltage, V_{cm} (voltage between the subject's body and differential amplifier common terminal), which can thereby introduce interference in bio-potential amplifiers. Most of the existing designs of the wall power supplied EEG systems use driven right leg (DRL) circuit to attenuate this common mode power-line interference in EEG recordings [18–22]. DRL circuits are being used for over 50 years to reduce V_{cm} interference and to provide patient safety [23]. The objective of the DRL circuit is to collect the common mode signals from all the EEG channels, invert and amplify them, then feed it back to the subject using a separate electrode generally known as DRL electrode. However, since 1967, amplifier common and earth ground are mandated to be electrically isolated from wall power supply, therefore, it ensures patient's safety [24].

Though DRL circuits have proven to be useful for wall power supplied bio-potential amplifiers, their significance for battery-powered EEG systems has not been thoroughly examined. We examine the need for DRL scheme in the context of battery-powered

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wearable EEG systems with the availability of high-performance COTS instrument amplifiers. The focus of this study is to evaluate if battery-powered EEG systems can work reasonably without DRL circuit. The intuition lies in the fact that (a) for battery-powered devices that are fully disconnected from the wall power supply, the concerns for the flow of dangerous line currents and large voltage build up on the human subject are not substantial. (b) V_{cm} is also significantly small for battery-powered fully wireless ambulatory and wearable devices because Cs (stray capacitance between the amplifier common and earth ground) is a few order smaller (pF range) than the typical value given in [25] for wall power supplied devices. Thus, the prime reason to use DRL circuit in battery-powered EEG devices is the mitigation of power-line interference (e.g. 60 Hz for the USA). We hypothesize that this interference can be dealt with carefully designed filters in the Analog Front End (AFE) in combination with availability of instrumentation amplifiers (inst-amp) with high Common Mode Rejection Ratio (CMRR). Therefore, for battery-powered EEG systems, we postulate that the significance of DRL circuit needs to be comprehensively investigated.

A major motivation to eliminate DRL for battery powered systems is to develop modular and scalable EEG systems. DRL circuit prohibits modularization of EEG systems. If battery-powered DRL-less EEG systems can be designed for each channel independently, then a Lego-like EEG system [26] with a unconstrained number of channels can be designed compared to conventional fixed number of channel based EEG systems [27–29]. In this work, we investigate the effect of DRL circuit elimination by customizing a single-channel AFE for an EEG system that can be operated with and without DRL circuit, and present the performance comparison. To the best of our knowledge, such study on investigating the impact of DRL in battery-powered EEG has not been reported in the literature.

2. "DRL-less AFE for battery-powered EEG

This section explains the objectives of using DRL circuit in the conventional wall-powered EEG. The concept of a novel AFE for battery-powered EEG is also proposed which can measure brain signals without using DRL circuit.

2.1. Concept of the DRL circuit

The common mode voltage V_{cm} (voltage of the human subject with respect to the differential amplifier's common), as shown in Fig. 1, occurs due to the displacement current (i_d) coupled to the subject because of the electromagnetic field through the subject to earth; power lines being earth grounded [30]. It is important to minimize V_{cm}, as it is an interfering noise to EEG signals [31]. Mathematically, V_{cm} is calculated, as explained in [25], as:

$$V_{cm} = R_c i_{d2} \tag{1}$$

$$R_c = \frac{R_{e1}}{G+1} \tag{2}$$

$$\text{Gain of DRL amplifier,} \quad G = \frac{2R_f}{R_a} \tag{3}$$

and

$$i_{d2} = \frac{i_d C_s}{C_s + C_b} \tag{4}$$

where R_{e1} and R_{e2} represent the electrode resistances, R_o is the current limiting resistor and R_f is the feedback resistor. D_1 is the differential amplifier to sense the differential electrode voltage. C_b and C_s represent the capacitance between body and earth ground (100 pF to 1 nF), and the stray capacitor between the amplifier common and earth ground respectively. Resistor R_a senses V_{cm} by averaging differential voltage of the electrode pair. Amplifier A_3 amplifies and inverts the sensed voltage V_{cm} and feeds it back to the subject through the DRL electrode.

As outlined in [25], the prime motives of DRL are to eradicate (a) hazardous line current that might flow through the ground loop, and (b) high voltage developed on patient because of the poor impedance of the connected electrode. For low-voltage battery-powered devices, which are fully disconnected from wall-power supply, these rationales are irrelevant as there is no ground loop and, in the case of any fault, the voltage at the electrodes will be limited by the safe battery voltage (e.g. 3.7 V for LiPo).

Furthermore, for the battery-powered devices, C_s is very small compared to wall-powered devices. Thus, the discharge current i_{d2} as given in Eqs. (1) and (4) also becomes negligibly small. This drastically reduces V_{cm} leading to compromise the motive of DRL circuit to minimize V_{cm}. In addition, DRL circuit might increase differential mode noise if not properly matched [30].

2.2. Novelty of the proposed "DRL-less" AFE

In contrast to the conventional approach of reducing interfering noise using DRL, we propose to eliminate the common mode power-line interference with a carefully designed AFE circuit for EEG systems. In our proposed AFE configuration, we have used a differential amplifier with high CMRR followed by a high-Q active notch filter to minimize the power-line RF interference [32]. Inserting a notch filter immediately after the instrumentation amplifier prior to the substantial amplification of the signal further helps in improving the Noise Figure (NF).

$$\text{NF} = \frac{P_{\text{sig}}/N_s}{GP_{\text{sig}}/(GN_s + N_{\text{amp,o}})} = 1 + \frac{N_{\text{amp},i}}{N_s} \geqslant 1 \tag{5}$$

Here noise in the input signal is N_s, P_{sig} is the power of the signal, G is the gain of the amplifier stage, noise introduced by the amplifier stage is $N_{\text{amp,o}}$ and $N_{amp,i} = N_{amp,o}/G$ is called input referred noise. Due to the input referred noise, any stage of a cascaded amplifier will introduce additional noise as given in (5). Hence, noise suppression is more effective at an earlier stage. For example, for a two-stage cascaded system (denoted by subscripts 1 and 2), the overall noise figure [33] is expressed as:

$$\text{NF}_{\text{overall}} = \text{NF}_1 + \frac{\text{NF}_2 - 1}{G_1} \tag{6}$$

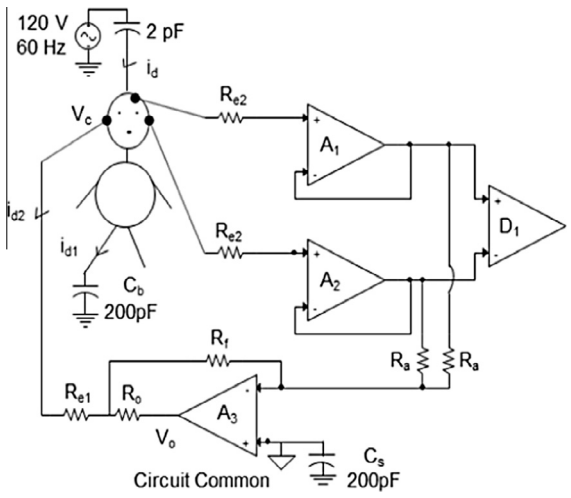

Fig. 1. A common EEG DRL circuit scheme (using op-amp A_3) depicting the power-line interference coupling in amplifiers adopted from [25].

Improving NF_1 is more effective than improving NF_2 by a factor of G_1 (refer (6)), thus we have inserted notch filter immediately after the instrument amplifier.

Based on these considerations, a 2-channel referential montage based ambulatory DRL-less EEG system was previously designed, prototyped, and evaluated. The device (''*NeuroMonitor*'') was able to successfully record brain activities in real-life settings [32,34]. The temporal and spectral responses of *NeuroMonitor* was also compared with a commercially available DRL based *Neuroscan* EEG system. The results showed that the signals from the two devices are very comparable despite the role of DRL in the later device [35]. These experiments encouraged us to investigate the effect of elimination of DRL in battery-powered EEG systems.

3. Methods for analysis

This section discusses in detail about the circuit design of the DRL circuit, customized single-channel EEG system, and the measurement set up used in this study to evaluate common-mode and power-line interference.

3.1. AFE of single-channel EEG

The designed analog front end of single channel EEG device is based on referential montage i.e. difference between the CH1 electrode (physically connected with any frontal lobe location) and Ref electrode (physically connected to mastoid/ear lobe) is measured. The AFE of the device under test (DUT) consists of INA 118 inst-amp (gain = 26) followed immediately by a Twin-T notch filter f_c = 60 Hz (−28 dB attenuation) to cope up with power-line interference (as per USA standard). The input to AFE is measured with respect to V_{gnd}, which avoids any issue related to DC offset from the electrode. AFE also consists of 2nd-order Butterworth low-pass filter followed by a passive low pass filter with f_c = 47.5 Hz (gain = 1.61) and a high pass filter with f_c = 0.16 Hz (gain = 0.83). After filtering, signals are biased at the mid-rail to avoid any static offset within the circuitry and passed through a final amplification stage of the op-amp (gain = 17.5). The total expected differential gain of the AFE, A_v is 608 (or 55.67 dB) for the frequency ranges of 0.16 Hz to 47.5 Hz.

All the op-amps used in the AFE design are AD8607 (Analog Devices, Inc., Norwood, MA), which is a dual channel rail-to-rail input and output amplifier with a very low offset, low noise (22 nV/$\sqrt{}$Hz) and very low input bias current (1 pA max.). This miniature, high-precision (patented trimming technique) and micro power op-amp with a typical CMRR of 100 dB is a suitable choice for portable battery-powered EEG systems. The AFE circuitry uses unipolar input supply of 3.3 V with its output referenced to virtual ground (V_{gnd}) at mid-rail 1.65 V. A voltage divider circuit followed by the buffer is designed to provide V_{gnd} supply to the DUT. The EEG prototype boards are designed using Allegro PCB designer (Cadence Design Systems, Inc., CA, USA) and fabricated through a commercial PCB foundry (OSH Park, OR, USA).

Some of the key features of the proposed novel ''DRL-less'' AFE are recapitulated below:

1. The first stage of the AFE contains a low gain, high CMRR (around 110 dB) inst-amp to avoid the saturation of the amplifier due to changes in the input differential signals that can include high amplitude artifacts and baseline wandering drift.
2. A unity gain active notch-filter is placed next to the inst-amp to mitigate the interference effect at the early stages of instrumentation and improve the overall noise figure.
3. To combat with the baseline drift, a DC biasing circuit is placed before the final stage of amplification which keeps the signal close to the ADC midrange.
4. The amplifier at the last stage amplifies the signal adequately after the DC offset (if any) elimination to utilize the full dynamic range of ADC.

3.2. DRL circuit design

For this study, a prototype four-layer Printed Circuit Board (PCB) was developed with only AFE capabilities on it. Here, we consider referential montage, however, performance is not dependent on the montage selection. As shown in Fig. 1, the typical DRL circuit (implemented with A3) is an inverting feedback circuit which in order to reduce the common mode noise of the electrodes, feeds the inverse of common-mode voltage back to the subject [36]. In this study, a similar DRL circuit is designed (Fig. 2). For the case of AFE without DRL, virtual ground (V_{gnd}), which is at the mid-rail between V_{dd} and GND, replaces DRL electrode.

EEG signals recorded from the scalp are very small in amplitude (within 100 μV range), which necessitate extremely low-noise differential mode amplification and high input impedance amplifier. INA118 (Texas Instruments Inc., TX, USA) inst-amp was used to amplify the difference between signals from CH1 and Ref EEG electrodes. This inst-amp offers a high common mode rejection ratio (CMRR) up to 110 dB, which helps in rejecting the common-mode noise at both inputs. Beside of its high CMRR, INA118 is an excellent choice for the analog front end circuit design because it is laser-trimmed for very low offset voltage (50 μV max.) and low drift (0.5 μV/°C). It can also operate with power supplies as low as ±1.35 V with a very low quiescent current (350 μA) which makes it ideal for battery-powered EEG devices.

INA118 senses V_{cm} and gives it to the voltage follower, designed using an AD8607 operational amplifier (op-amp). The voltage follower/buffer in the design has unity gain and low output impedance, thus, it behaves as a perfect voltage source. The last stage of the DRL circuit consists of an inverting op-amp. The output signal of DRL circuit (DRL OUT in the schematic) is thus inverted and amplified as compared to V_{cm} and is fed back to the subject using the DRL electrode.

3.3. Experimental setup to analyze common mode interference

Common mode voltage between subject's body and the amplifier common can cause interference in the input of the differential amplifier. To evaluate these interference in the customized DUT, CMRR has been calculated experimentally (with and without DRL). Mathematically, the output, V_{out} of the DUT as shown in Fig. 3 can be defined in terms of differential mode voltage (V_{dm}) and common mode voltage (V_{cm}) as below:

$$V_{dm} = V_2 - V_1 \tag{7}$$

$$V_{cm} = \frac{V_2 + V_1}{2} \tag{8}$$

$$V_{out} = V_{cm}A_{cm} + V_{dm}A_{dm} \tag{9}$$

where A_{cm} and A_{dm} represents common mode gain and differential mode gain respectively. CMRR (in dB) of the DUT is thereby measured as:

$$\text{CMRR} = 20\log_{10}\left|\frac{A_{dm}}{A_{cm}}\right| \quad \text{dB} \tag{10}$$

By substituting the values of V_{cm} in Eq. (9), differential mode gain A_{dm}, for both DRL and without DRL conditions are measured as:

$$A_{dm} = \frac{V_{out}}{V_{dm}} \tag{11}$$

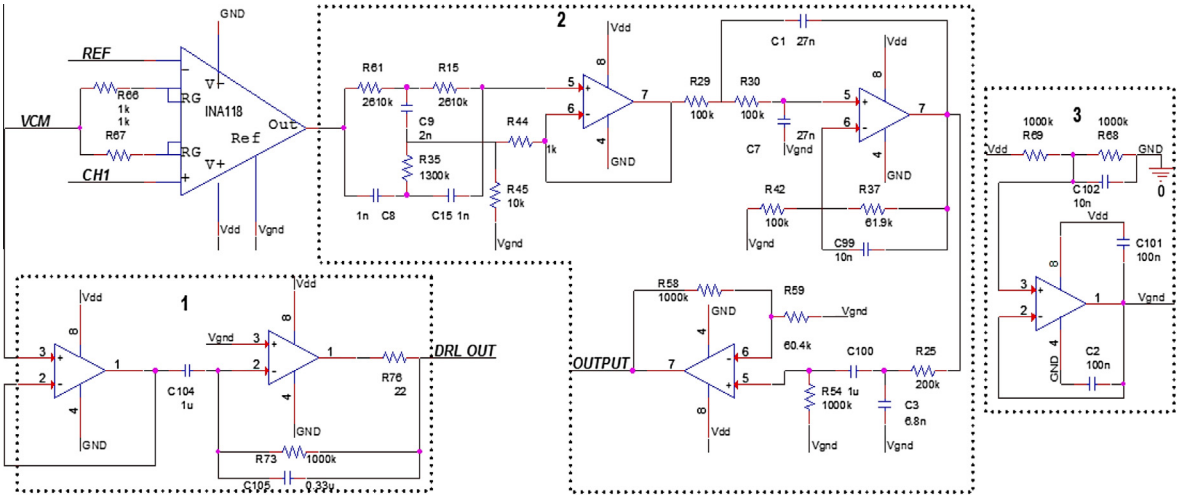

Fig. 2. Schematic of the single-channel referential montage EEG acquisition circuit (Device under test) using Instrumentation amplifier (INA118). Legends (1) DRL circuit. (2) Analog filters (Notch, low pass and high pass filters). (3) Virtual ground supply. For EEG circuit without DRL circuit, the V_{gnd} terminal was connected to the corresponding electrode.

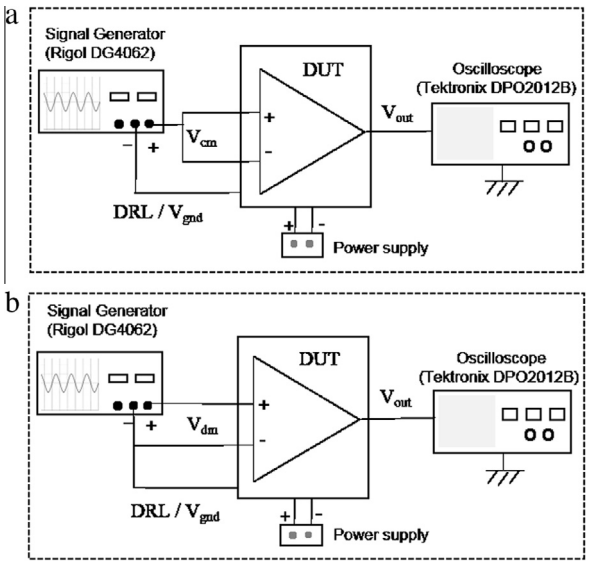

Fig. 3. Set up of the DUT to calculate the CMRR with and without DRL circuit. Connections for measuring. (a) Common mode gain. (b) Differential mode gain. Either V_{gnd} or DRL electrode is connected to the DUT based on the measurement without and with DRL circuit respectively.

Similarly, common-mode gain A_{cm}, for DRL and without DRL conditions can thereby be measured as:

$$A_{cm} = \frac{V_{out}}{V_{cm}} \tag{12}$$

4. Experimental results

The custom-designed battery-powered single-channel EEG (refer Fig. 4) is used in this study for the DRL investigation. EEG signals are recorded using the Pre-gelled Ag/AgCl GS-26 electrodes (Bio-medical Instruments Inc., MI, USA) placed on the prefrontal cortex (FP2) and right mastoid. The third electrode on the left mastoid could be connected to either the output of the DRL circuit (when using DRL circuit) or to inst-amp common V_{gnd} (when not using DRL circuit). The analog EEG signals are measured using a DSOX2024A digital oscilloscope (Agilent Tech., CA, USA). In Fig. 5, Fast Fourier Transform (FFT) of the output signal (computed using rectangular windowing technique in Tektronix DPO2012B oscilloscope) when acquired using DRL and without DRL circuit are plotted. Here, the test input signal, a sine wave with amplitude, V_{in} = 4 $mV_{p\text{-}p}$, at a representative EEG signal frequency of 20 Hz and utility line-frequency of 60 Hz (for the USA) is used. The plot depicts that the signals obtained with and without DRL are very similar to each other in amplitude even at the 60 Hz line-frequency.

Though the notch filter for this study is designed for 60 Hz (for US based EEG systems), similar results are expected when the filter is tuned to 50 Hz (for European based EEG systems).

Further, we evaluate the CMRR of the DUT to better understand the extent of suppressing the common mode interference in our custom AFE. We compute the differential mode output, V_{out} of the system for the given input at 20 Hz and 60 Hz. The physical connection of DUT to measure the common mode and differential mode gain is as represented in Fig. 3. The output of DUT, V_{out} connects to an ADA400A differential preamplifier (Tektronix, Inc., Bracknell, UK), which due to its high gain, selectable bandwidth and extremely high common mode rejection, allows the measurements of very low amplitude voltage signals even in high-noise environments. This preamplifier further allows direct output measurement with Tektronix DPO2012B oscilloscope. It can be interpreted from the tabulated results in Table 1 that for the given V_{dm} input at 20 Hz, V_{out} for both conditions (DRL and without DRL) remains similar. Also, for V_{dm} input at 60 Hz there is insignificant difference between V_{out} of DRL and without DRL conditions, refer Table 2. This signifies that the designed DUT is robust for mitigating differential-mode interference at power-line frequency even without using DRL circuit. To find the common mode output (V_{out}) tabulated in Tables 3 and 4, two inputs of the ins-amp are shorted and V_{cm} is applied to the input. We note that for very small common mode input voltage, the output voltage is noisy which might be because of low Signal to Noise ratio. Also, for V_{cm} > 400 - mV the output voltage for both cases (with and without DRL), is bit distorted as the DUT exceeds its linearity range. From the table's data (for 20 Hz and 60 Hz, with and without DRL), V_{dm} is plotted against V_{out} in Fig. 6 and linear regression is performed. The slope of V_{dm} vs. V_{out} is the measure of common mode and differential mode voltages with respect to the output voltage with the fitted linear trend line and coefficient of determination R^2 written next of each trend line (refer Fig. 6). Based on the slope values obtained

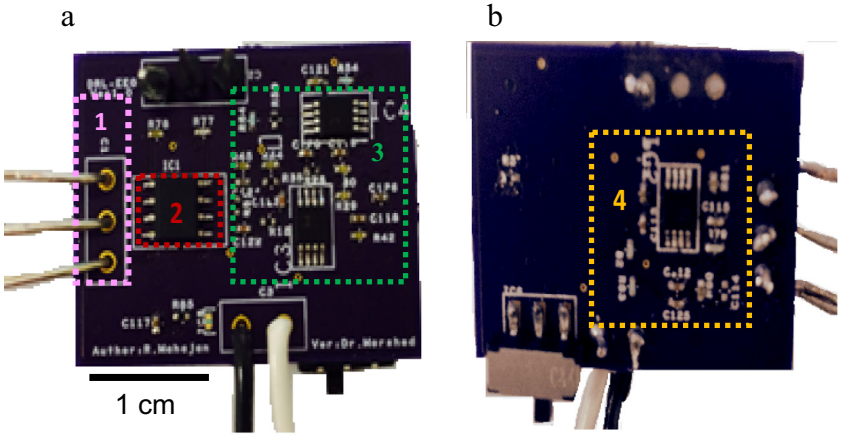

Fig. 4. PCB of the custom designed EEG system (DUT) to analyze DRL paradigm. (a) Top view of the PCB. (b) Bottom view of the PCB. Legends: (1) Channel electrodes (2) INA 118 instrument amplifier. (3) AFE. (4) DRL amplifier.

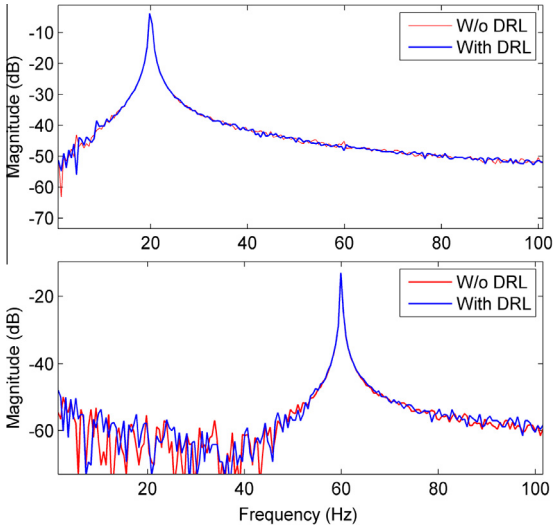

Fig. 5. FFT of the DUT's output signal for the input sinusoidal signal, V_{in} = 4 $mV_{p\text{-}p}$ at (Top) 20 Hz (Bottom) 60 Hz with and without DRL circuit.

Table 1
A_{dm} computed with 20 Hz input signal.

V_{dm} (mV)	V_{cm}	$V_{out(DRL)}$ (V)	$V_{out(w/o\ DRL)}$ (V)	$A_{dm(DRL)}$	$A_{dm(w/o\ DRL)}$
2.0	0	1.24	1.40	620.0	700.0
2.5	0	1.48	1.52	592.0	608.0
3.0	0	1.80	1.80	600.0	600.0
3.5	0	2.12	2.12	605.7	605.7
4.0	0	2.44	2.44	610.0	610.0
4.5	0	2.80	2.80	622.2	622.2
5.0	0	3.00	3.00	600.0	600.0

Table 2
A_{dm} computed with 60 Hz input signal.

V_{dm} (mV)	V_{cm}	$V_{out(DRL)}$ (mV)	$V_{out(w/o\ DRL)}$ (mV)	$A_{dm(DRL)}$	$A_{dm(w/o\ DRL)}$
2.0	0	380	380	190	190
2.5	0	440	460	176	184
3.0	0	540	540	180	180
3.5	0	620	620	177	177
4.0	0	700	700	175	175
4.5	0	780	780	173	173
5.0	0	880	880	176	176

Table 3
A_{cm} computed with 20 Hz input signal.

V_{dm}	V_{cm} (mV)	$V_{out(DRL)}$ (mV)	$V_{out(w/o\ DRL)}$ (mV)	$A_{cm(DRL)}$	$A_{cm(w/o\ DRL)}$
0	20	6*	6*	0.300	0.300
0	40	8	8	0.200	0.200
0	100	18	22	0.180	0.220
0	200	34	34	0.170	0.170
0	400	58**	66**	0.145	0.165
0	800	118**	132**	0.148	0.165

Table 4
A_{cm} computed with 60 Hz input signal.

V_{dm}	V_{cm} (mV)	$V_{out(DRL)}$ (mV)	$V_{out(w/o\ DRL)}$ (mV)	$A_{cm(DRL)}$	$A_{cm(w/o\ DRL)}$
0	20	2.40*	2.40*	0.12	0.12
0	40	3.40	3.20	0.09	0.08
0	100	5.40	5.76	0.05	0.06
0	200	8.60	10.80	0.04	0.05
0	400	15.60**	20.00**	0.04	0.05
0	800	32.00**	35.20**	0.04	0.04

* Noise observed.
** Distortion observed.

from the plots, V_{cm} and V_{dm} input–output voltage relationship of the DUT can be described as given in the expressions below. For input signal at 20 Hz:

$$V_{out(\text{with DRL})} = 0.1427V_{cm} + 611.43V_{dm} \quad (13)$$

$$V_{out(\text{w/o DRL})} = 0.1608V_{cm} + 571.43V_{dm} \quad (14)$$

Therefore using (10), CMRR at 20 Hz input signal is found as:

$$\text{CMRR}_{\text{with DRL}} = 20\log_{10}\left|\frac{611.43}{0.1427}\right| = 72.64\,dB \quad (15)$$

$$\text{CMRR}_{\text{w/o DRL}} = 20\log_{10}\left|\frac{571.43}{0.1608}\right| = 71.01\,dB \quad (16)$$

Similarly for input signal at 60 Hz, CMRR of DUT can be calculated as:

$$V_{out(\text{with DRL})} = 0.0375V_{cm} + 167.14V_{dm} \quad (17)$$

$$V_{out(\text{w/o DRL})} = 0.0425V_{cm} + 164.29V_{dm} \quad (18)$$

$$\text{CMRR}_{\text{with DRL}} = 20\log_{10}\left|\frac{167.14}{0.0375}\right| = 72.98\,dB \quad (19)$$

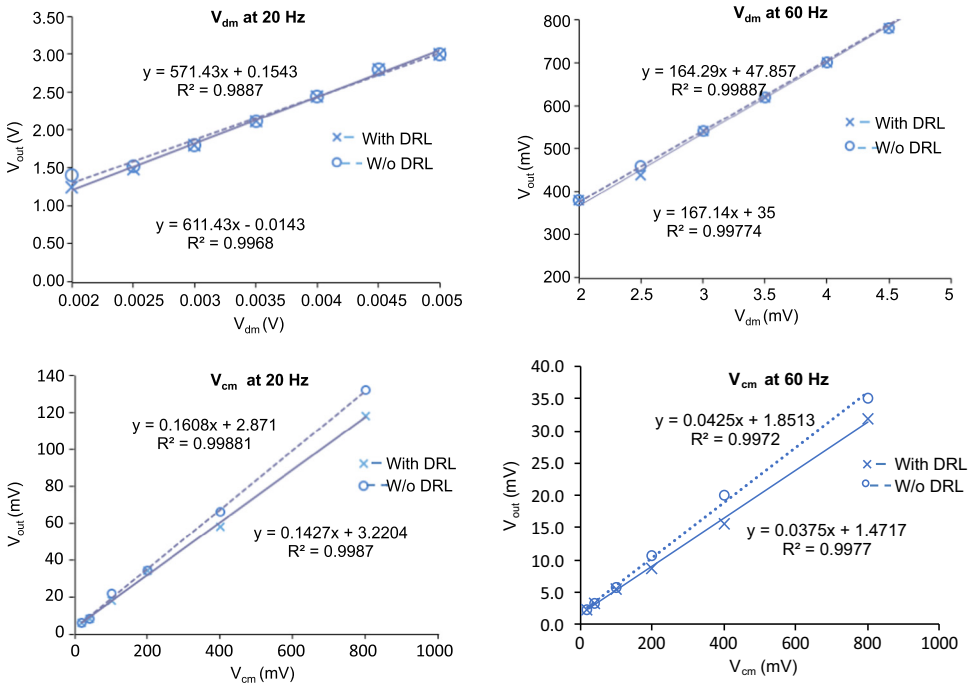

Fig. 6. Comparison plots for calculating the CMRR of the DUT implemented with and without DRL circuit. (Top) V_{dm} vs. V_{out} plot for experimental differential mode gain. (Bottom) V_{cm} vs. V_{out} plot for experimental common mode gain, both computed at 20 Hz and 60 Hz. The linear trend line is represented by the equation $y = m * x + c$, where m is the slope and c is the y-intercept.

$$\mathrm{CMRR}_{\mathrm{w/o\ DRL}} = 20\log_{10}\left|\frac{164.29}{0.0425}\right| = 71.74\,dB \tag{20}$$

The experimental CMRR of the designed DUT for input signal at 20 Hz and 60 Hz is higher than the typical value in the literature [37]. The observed CMRR is also in-line with International Federation of Clinical Neurophysiology (IFCN) standards for measuring EEG signals [38]. Also, at both frequencies CMRR differs insignificantly when recorded with or without DRL circuit with our AFE, compared to 40–50 dB expected difference as reported in the literature [39]. These results suggest the importance of DRL circuit in our battery-powered EEG with the designed AFE is dubious.

Further, actual EEG data is recorded from 3 subjects with the Ch1 electrode connected at the frontal lobe location (FP2), reference electrode at the right mastoid and a third electrode either with DRL output or with V_{gnd} (output is measured using an Agilent oscilloscope, refer Fig. 7). To get a better understanding of the behavior of DUT, EEG signals are continuously recorded for about 30 s from each subject during different environmental conditions like during walk, while sitting idle on the chair with eyes closed, touching a conductive object and touching a grounded object. Fig. 8 shows EEG signal of 8 s duration from Subject 1 during normal walking condition while DUT is connected with and without DRL. Two eye-blinks can be seen conspicuously between 4 and 7 s for both conditions. Fig. 9 represents the continuous EEG signal for ~27 s with Subject 1 for three different conditions. The time-domain signals for DRL and without DRL conditions are qualitatively comparable. For frequency-domain comparison, Power Spectral Density (PSD) of the recorded EEG data is computed using pwelch function in MATLAB (MathWorks, MA, USA) with Hamming window of length 200 over FFT length of 1024 with 50% window overlap. PSD plot in Fig. 10 suggest that at 60 Hz there is a maximum difference of 1 dB with and without DRL circuit for Subject 1, ~4 dB for Subject 2 and ~2 dB for Subject 3.

As evident, the improvement of interference removal using DRL circuit is insignificant compared to the proposed DRL-less AFE for EEG system. These results suggest that the DRL circuit can be eliminated using our proposed AFE design without incurring significant impact on the EEG signal quality.

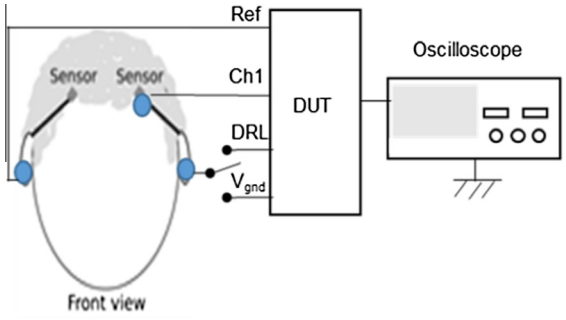

Fig. 7. Connection setup with the DUT to record EEG signal using CH1 electrode. Electrode at the mastoid is either connected to DRL when DRL circuit is used for the experiment or to the V_{gnd}.

5. Discussion

The traditional design of wall-powered EEG systems uses DRL circuit to reject the common mode noise and power-line interference. DRL circuit prohibits modularity for EEG systems as its circuit design substantially depends upon the number of EEG channels to be used (refer Fig. 1). Therefore, in a case of an inclusion or exclusion of the channel, DRL circuit needs to be redesigned. This makes the DRL based EEG system to have fixed, non-reconfigurable number of channels. Elimination of DRL as suggested in this study with the proposed AFE design not only reduces the complexity of the entire system but also allows for modular structure of EEG system [40]. Further, it reduces the power requirement for the dedicated DRL circuitry, which can be critical for the long-term monitoring applications with battery-powered systems.

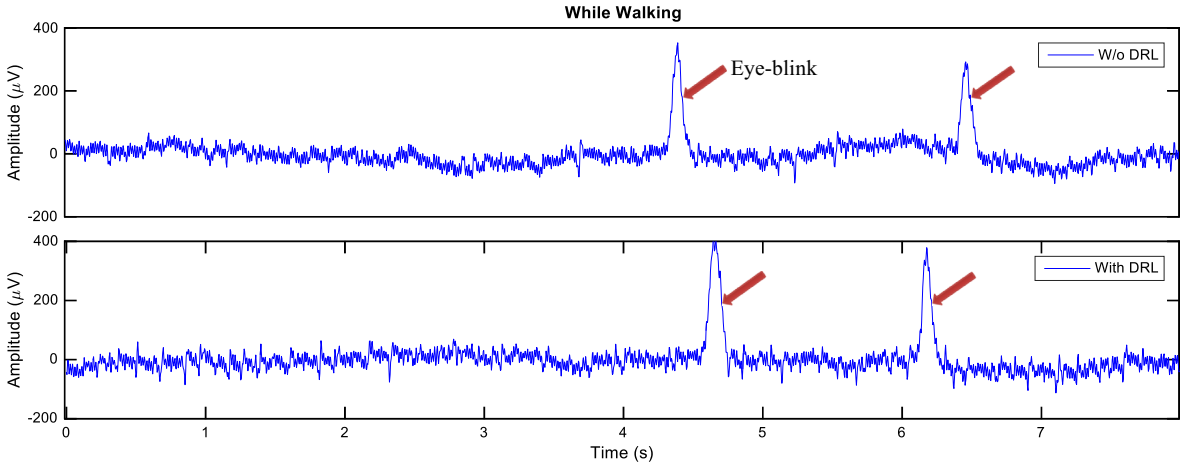

Fig. 8. EEG signals recorded from FP2 location when Subject 1 was walking while DUT connected with and without DRL.

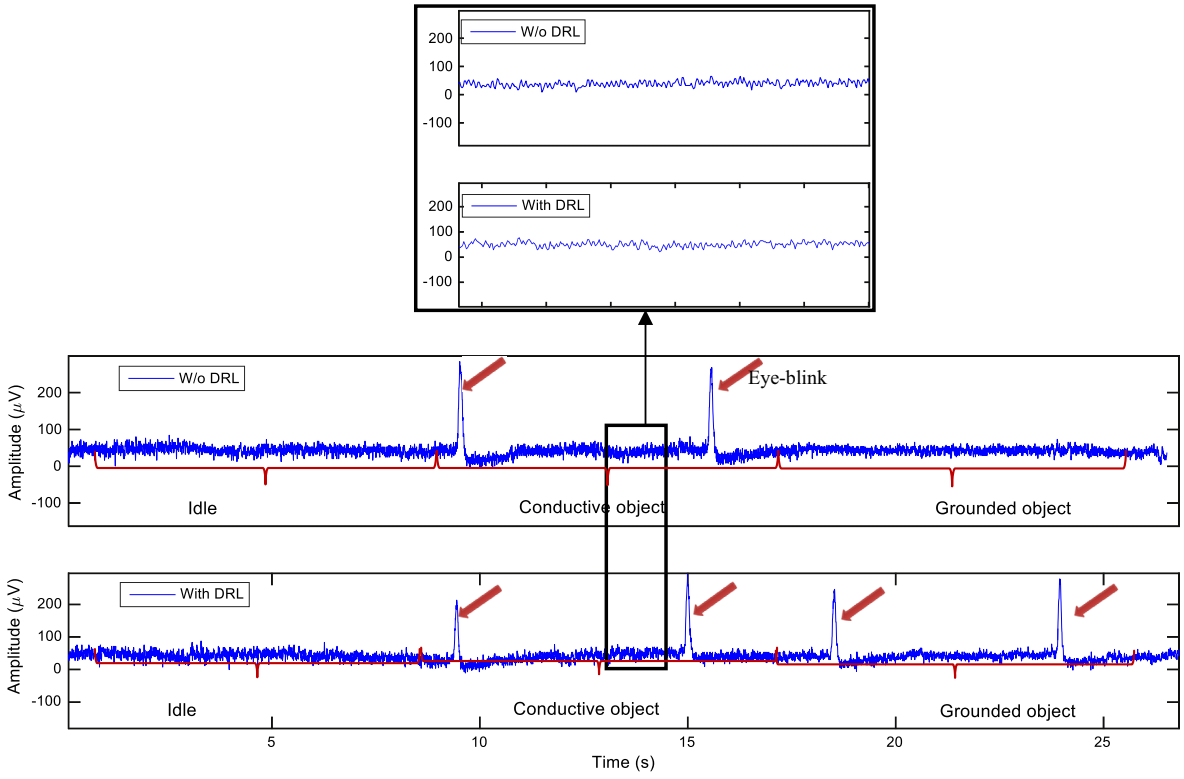

Fig. 9. EEG signals recorded when Subject 1 sits idle on the chair, touches a conductive object and touches a grounded object.

The notch filter in this study is designed on the basis of 60 Hz line-frequency in the USA, but the filter can be modified for European EEG systems. We understand that the notch filter will suppress some neuronal signals at 60 Hz due to spectral overlap; however, use of that specific frequency for neuroscience applications are scarce.

The PSD data show some reminiscent 60 Hz interference for both cases (with and without DRL), which can be due to component tolerances (±5%). This can be improved by employing higher tolerance components as well as by utilizing a more complex notch filter. However, this study focuses on comparing performances with and without DRL for common mode signals (e.g. power line interference at 60 Hz). Note that the key advantage with the proposed DRL-less design is that each EEG channel is independent; hence, any number of these independent channels can be connected at the deployment time in a plug-and-play fashion.

Though this study focuses on the DRL analysis with EEG, similar effects on DRL elimination are expected using the proposed AFE for other bioelectric instrumentation systems, like Electrocardiogram (ECG).

6. Conclusion

EEG is a suitable non-invasive technology to reliably capture brain signals at natural environment, but has intricate challenges prohibiting modularization, such as driven-right-leg (DRL) circuit requirement. In this study, we evaluate the performance of a novel DRL-less single-channel AFE design for battery-powered wearable

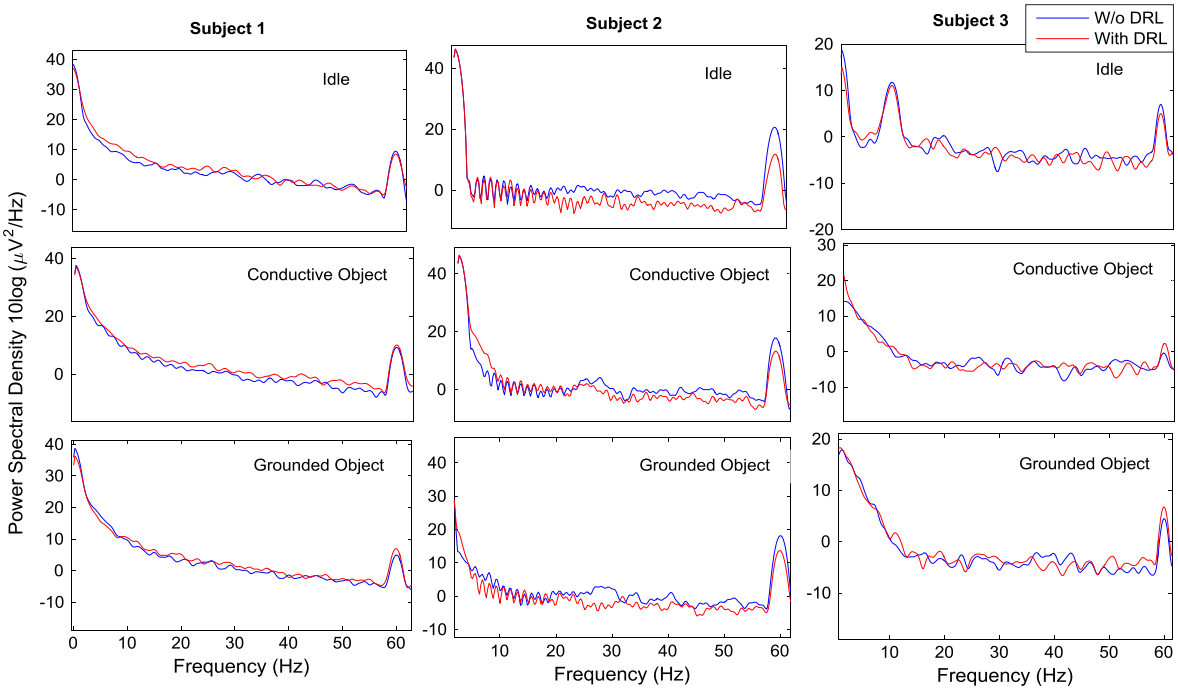

Fig. 10. PSD of the recorded EEG signals from 3 Subjects from FP2 location for three experimental conditions-sitting idle, touching conductive object and touching grounded object.

EEG system. Comparative data were presented for EEG with and without DRL circuit. Results have shown that the designed EEG with the proposed AFE offers CMRR of 72.64 dB (at 20 Hz) and 72.98 dB (at 60 Hz) when using DRL circuit, and 71.01 dB (at 20 Hz) and 71.74 dB (at 60 Hz) without using DRL circuit. As observed with the time-domain and frequency-domain results, DRL circuit did not contribute significantly for performance improvement of the EEG system (<4 dB for the test cases). Hence, elimination of DRL for battery powered ambulatory system, wearable EEG, might greatly simplify AFE design, interdependency of circuit design for multichannel EEG system, and complexity on deployment, and thus pave the path for a modular and scalable design of battery-powered wearable EEG systems.

Ethical approval

This study involves data acquisition from the human subjects and was therefore pre-approved by the Institutional Review Board of the University of Memphis (Approval number: 2289).

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References

[1] B. He et al., Grand challenges in mapping the human brain: NSF workshop report, IEEE Trans. Biomed. Eng. 60 (11) (2013) 2983–2992.
[2] B.I. Morshed, A. Khan, A brief review of technologies and challenges to monitor brain activities, J. Bioeng. Biomed. Sci. 4 (1) (2014) 1–10.
[3] C. Lin et al., Noninvasive neural prosthesis using mobile and wireless EEG, Proc. IEEE 96 (7) (2008) 1167–1183.
[4] P. Mohseni, K. Najafi, A wireless FM multichannel microsystem for biomedical neural recording applications, Proc. IEEE South-west Symp. Mixed Signal Design, Tucson, AZ, Feb. 23–25, 2003, pp. 217–222.
[5] P. Mohseni, K. Najafi, Wireless multichannel biopotential recording using an integrated FM telemetry circuit, Proc. 26th Annual Int. Conf. Engineering in Medicine and Biology Soc., San Francisco, CA, Sep. 1–4, 2004, pp. 4083–4086.
[6] P. Mohseni, K. Najafi, A battery-powered 8-channel wireless FM IC for biopotential recording applications, Dig. Tech. Papers 2005 IEEE Int. Solid-State Circuits Conf., San Francisco, CA, Feb. 6–10, 2005, pp. 560–561.
[7] I. Obeid, M.A.L. Nicolelis, P.D. Wolf, A multichannel telemetry system for single unit neural recordings, J. Neurosci. Meth. 133 (2004) 123–135.
[8] S. Farshchi et al., A tinyOS-enabled MICA2-based wireless neural interface, IEEE Trans. Biomed. Eng. 53 (7) (2006) 1416–1424.
[9] R. Matthews et al., A wearable physiological sensor suite for unobtrusive monitoring of physiological and cognitive state, in: 29th Annual International Conference of the IEEE EMBS, 2007, pp. 5276–5281.
[10] M.K. Hazrati et al., Wireless brain signal recordings based on capacitive electrodes, in: IEEE 8th International Symposium on Intelligent Signal Processing, 2013, pp. 8–13.
[11] Y.M. Chi et al., Wireless non-contact cardiac and neural monitoring, Wireless Health (2010) 15–23.
[12] Xiaodan Zou, W.-S. Liew, Libin Yao, Yong Lian, A 1V 22μW 32-channel implantable EEG recording IC, in: IEEE International Solid-State Circuits Conference, 2010, pp. 126–127.
[13] Lin Zhu et al., Design of portable multi-channel EEG signal acquisition system, in: 2nd Intl Conf on BioMedical Engineering and Informatics, Tianjin, China, 2009, pp. 1–4 (October).
[14] S. Debener, F. Minow, R. Emkes, K. Gandras, M. de Vos, How about taking a low-cost, small, and wireless EEG for a walk?, Psychophysiology 49 (11) (2012) 1617–1621
[15] Y.M. Chi, T. Jung, G. Cauwenberghs, Dry-contact and noncontact biopotential electrodes: methodological review, IEEE Rev. Biomed. Eng. 3 (2010) 106–119.
[16] R. Schuyler, A. White, K. Staley, K.J. Cios, Epileptic seizure detection, IEEE Eng. Med. Biol. Mag. 26 (2) (2007) 74–81.
[17] C. Lin et al., Noninvasive neural prostheses using mobile and wireless EEG, Proc. IEEE 96 (7) (2008) 1167–1183.
[18] M. Engin et al., A prototype portable system for EEG measurements, Measurement 40 (9) (2007) 936–942.
[19] S.D. Ridwan et al., Single channel wireless EEG: Proposed application in train drivers, in: 3rd IEEE International Conference on Broadband Communications, Information Technology & Biomedical Applications, 2008, pp. 58–63.
[20] X. Chen, J. Wang, Design and implementation of a wearable, wireless EEG recording system, in: 5th IEEE International Conference on Bioinformatics and Biomedical Engineering, 2011, pp. 1–4.
[21] Manj. Benning, The Experimental Portable EEG/EMG Amplifier PhD diss., University of Victoria, 2003.
[22] P.S. Pandian et al., Low noise multi-channel biopotential wireless data acquisition system for dry electrodes, in: 15th International Symposium on: Smart Structures and Materials & Nondestructive Evaluation and Health Monitoring, SPIE, 2008, pp. 69310Q-69310Q.

[23] J.C. Huhta, J.G. Webster, 60 Hz interference in electrocardiography, IEEE Trans. Biomed. Eng. BME-20 (2) (1973) 91–101.
[24] Patient safety, Med. Electro. Div., Hewlett-Packard Co., Waltham, Mass., Appl. Note, 1971, pp. 718.
[25] Bruce B. Winter, John G. Webster, Driven-right-leg circuit design, IEEE Trans. Biomed. Eng. BME 30 (1) (1983) 62–66.
[26] R. Mahajan, B.I. Moshed, Reconfigurable architecture for wearable sensor network, in: NIH-IEEE Strategic Conference on Healthcare Innovations and Point of Care Technologies for Precision Medicine (HI-POCT'15), Bethesda, MD, Paper MoPoster04.11, November 9th–10th, 2015.
[27] R.F. Yazicioglu, P. Merken, R. Puers, C.V. Hoof, A 200 μW eight-channel EEG acquisition ASIC for ambulatory EEG systems, IEEE J. Solid-State Circuits 43 (12) (2008) 3025–3038.
[28] J. Yoo, L. Yan, D. El-Damak, M.A. Altaf, A. Shoeb, A.P. Chandrakasan, An 8-channel scalable EEG acquisition SoC with fully integrated patient-specific seizure classification and recording processor, IEEE J. Solid-State Circuits 48 (1) (2013) 214–228.
[29] J. Xu, B. Busze, H. Kim, K.A.A. Makinwa, C. Van Hoof, R.F. Yazicioglu, A 60nV/$\sqrt{}$ Hz 15-channel digital active electrode system for portable biopotential signal acquisition, in: IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, February 2014, pp. 424–425.
[30] J. Gomez-Clapers, E. Serrano-Finetti, R. Casanella, R. Pallas-Areny, Can driven-right-leg circuits increase interference in ECG amplifiers? in: Annual Intl. Conf. of the IEEE EMBC, 2011, pp. 4780–4783.
[31] B.B. Winter, J.G. Webster, Reduction of interference due to common mode voltage in biopotential amplifiers, IEEE Trans. Biomed. Eng. BME 30 (1) (1983) 58–62.
[32] R. Mahajan, S. Consul-Pacareu, M.J. AbuSaude, M.N. Sahadat, B.I. Morshed, Ambulatory EEG neuromonitor platform for engagement studies of children with development delays, SPIE Proc. Smart Biomed. Physiol. Sensor Tech. X 8719 (2013) (87190L(1–10)).
[33] W. Namgoong, J. Lerdworatawee, Revisiting the noise figure design metric for digital communication receiver, Proc. Intl. Symp. Qual. Electron. Des. (2003) 159–162.
[34] S. Consul-Pacareu, R. Mahajan, M.N. Sahadat, B.I. Morshed, Wearable ambulatory 2-channel EEG neuromonitor platform for real-life engagement monitoring based on brain activities at the prefrontal cortex, in: Proceedings of the 2014 IAJC-ISAM International conference, 2014. ISBN 978-1-60643-379-9.
[35] R. Mahajan, C.A. Majmudar, S. Khatun, B.I. Morshed, G.M. Bidelman, NeuroMonitor ambulatory EEG device: comparative analysis and its application for cognitive load assessment, in: IEEE Healthcare Innovations and Point-of-Care Technologies Conf., Seattle, WA, 2014, pp. 133–136 (October).
[36] A.C. Metting Van Rijn, A. Pepper, C.A. Grimbergen, High quality recording of bioelectric events. Part I: interference reduction theory and practice, Med. Biol. Eng. Comput. 28 (1990) 389–397.
[37] T Zarifi, C.C. Peng, M.H. Zarifi, Low-power amplifier for in-vivo EEG signal recording, in: IEEE 1st Middle East Conference on Biomedical Engineering (MECBME), February 2011, pp. 19–22.
[38] M.R. Nuwer et al., IFCN standards for digital recording of clinical EEG, Electroencephalogr. Clin. Neurophysiol. 106 (3) (1998) 259–261.
[39] M. Guermandi et al., Active electrode IC combining EEG, electrical impedance tomography, continuous contact impedance measurement and power supply on a single wire, IEEE Proc. ESSCIRC (2011) 335–338.
[40] R. Mahajan, B.I. Morshed, G.M. Bidelman, Design and validation of a fully reconfigurable wearable EEG, in: 38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (accepted), Orlando, August 16–20, 2016.